Transparent Oxide TFTs Fabricated by Atomic Layer Deposition(FA2386-11-1-114052)

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Purpose and Background:

In recent years, the application of zinc oxide (ZnO) thin films as an active channel layer in TFTs has become of great interest owing to their specific characteristics. ZnO is transparent in the visible wavelengths region because of its wide band gap (~3.37eV), and the ability to fabricate good quality films over large areas at low temperature suggests the compatibility of ZnO films with plastic or other flexible substrates. Higher field-effect mobility of ZnO TFTs than a-Si:H TFTs has been recently demonstrated. However, reliability for electrical stress is one of serious problems in their mass production. An atomic layer deposition (ALD) method is one of the thin film fabrication technologies, which attracts much attention in LSI industry. The film deposited by ALD has additional features of accurate thickness control, high conformity, and uniformity over large areas, because of the alternating gas supply.

Approach:

To realize the high performance and reliable ZnO thin films transistors, we focused on atomic layer deposition. Previously we have established basic process condition for fabrication of ZnO film and thin film transistors. In this study, we will develop higher quality thin film and higher performance thin film transistors by using atomic layer deposition.

I. ALD deposition method

In this study, we will develop a new deposition method of high quality ZnO film by using ALD method. ALD thin films are deposited with alternating exposures of a source gas and an oxidant. General feature of the ALD method is as follows:

We will study ZnO thin films deposited by ALD. To control the carrier concentration in the films, we will propose plasma assisted ALD (PA-ALD) with oxygen radical as an oxidizer. The electrical and physical properties of the ZnO films are measured with and without annealing.

In this study, we will investigate ZnO thin films using PA-ALD to improve the ZnO TFT performance. The effects of preparation condition on the electrical properties are evaluated, and the effect of plasma condition on the quality of ZnO film is also investigated.

II. High Pressure vapor treatment

In order to improve the performance of ZnO thin film transistors, we will study the effect of High pressure vapor treatment on the performance and reliability. In the field of polycrystalline silicon TFTs, it is well known that the high pressure vapor treatment improve the mobility or threshold voltage. Previously we have revealed that the treatment oxidize the dangling bond at grain boundaries. In this study following points will be studied.

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14. ABSTRACT
To realize the high performance and reliable ZnO thin films transistors, we focused on atomic layer deposition. Previously we have established basic process condition for fabrication of ZnO film and thin film transistors. In this study, we will develop higher quality thin film and higher performance thin film transistors by using atomic layer deposition.

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TRANSPARENT OXIDE TFTS FABRICATED BY ATOMIC LAYER DEPOSITION (FA2386-11-1-114052)

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***Abstract*—Zinc oxide (ZnO) thin films have attracted significant attention for application in thin film transistors (TFTs) due to their specific characteristics, such as high mobility and transparency. The atomic layer deposition (ALD) thin film is deposited with alternating exposures of a source gas and oxidant. The ALD method keeps fabrication temperature of the ZnO TFTs low. In this study, we investigated the effects of the gate insulator properties on the performance of TFTs with a ZnO channel layer deposited by plasma-assisted ALD (PAALD). The TFTs with Al_2O_3 gate insulator indicated high performance (5.1 cm^2/Vs field effect mobility) without any thermal annealing. This result indicated a high-performance ZnO TFT with the films deposited by PAALD can be obtained at temperature below 100°C.**

I. INTRODUCTION

The most commonly used materials for the active channel layer in thin film transistors (TFTs) have been amorphous silicon (a-Si:H) and polycrystalline silicon (poly-Si).[1)] However, there are a number of drawbacks for these materials.[1-3] Whereas TFTs with the poly-Si channel layer have high mobility (>50 $cm^2V^{-1}s^{-1}$), a high-temperature process is needed for their fabrication. In addition, poly-Si is difficult to fabricate over large areas. [2] These issues make them incompatible with flexible substrates. On the other hand, a-Si:H is readily used in large-area flat panel displays. However, there are some limitations, such as low channel mobility (~1 $cm^2V^{-1}s^{-1}$) and the issues of degradation. [4] In recent years, the application of zinc oxide (ZnO) thin films as an active channel layer in TFTs has become of great interest owing to their specific characteristics. ZnO is transparent in the visible wavelength region because of its wide band gap (~3.37 eV), and the ability to fabricate good quality films over large areas at low temperature suggests the compatibility of ZnO films with plastic or other flexible substrates. [4-6] The higher field-effect mobility of ZnO TFTs than a-Si:H TFTs has recently been demonstrated. [4-9] However, the reliability against electrical stress is one of the serious problems in their mass production.

The atomic layer deposition (ALD) method is one of the thin-film fabrication technologies that attracts much attention in the LSI industry. Films deposited by ALD have the additional features of accurate thickness control, high conformity, and uniformity over large areas, because of the alternating gas supply. [10] Furthermore, it is reported that the TFTs with an ALD ZnO channel layer show high mobility. [11-13] However, undoped ZnO films grown by

ALD generally have unsuitable electrical properties such as high carrier concentration and high conductivity. [13] It is well known that the high carrier concentration of undoped ZnO films results from defects such as oxygen vacancies.

We have studied ZnO thin films deposited by ALD. To control the carrier concentration in the films, we proposed plasma-assisted ALD (PAALD) with oxygen radicals as an oxidizer. The electrical and physical properties of the ZnO films were measured with and without annealing. The TFTs with thePAALD ZnO film exhibited more excellent properties compared with the case of conventional ALD. Through our previous study, we found that the residual carrier concentration is reduced and high-performance ZnO TFTs are possible to obtain byPAALD at low temperature. [14, 15]

In this study, we prepared ZnO thin films for channel layers and Al_2O_3 for gate insulators using PAALD, and fabricated the bottom-gate type TFTs. For comparison, we adopted two kinds of materials as the gate insulator: thermally-oxidized SiO_2 (TO-SiO_2) and Al_2O_3 deposited by ALD. In order to reduce the operating voltage, high-*k* gate insulators are always used to increase the coupling of the gate electric field to the channel layer. The Al_2O_3 film is a high-*k* material that can be deposited at low temperature by ALD. TFTs with a TO-SiO_2 gate insulator were also fabricated for comparison.

II. EXPERIMENTAL METHODS

A. Atomic layer deposition

Atomic layer deposition is a method based on the sequential introduction of respective reaction precursors [8, 11] shown in Figs. 1(a) – 1(d). Sequential reactions can be designed when the product of the first surface reaction becomes a reactant for the second surface reaction. This results in layer-by-layer growth and full or partial monolayer deposition per precursor injection. Owing to the self-limiting surface reactions, thin films with high quality can be obtained with precise thickness control and excellent conformity over high surface area-to-volume ratio structures. In this method, only one reactant is present in the chamber at each procedure. This prevents any unwanted gas phase reactions observed in the chemical vapor deposition method, which can lead to particle formation and inferior device performance. In particular, ALD can produce high-quality films at relatively low temperatures, which makes it very attractive for the active channel layer deposition of TFTs on plastic or flexible substrates.

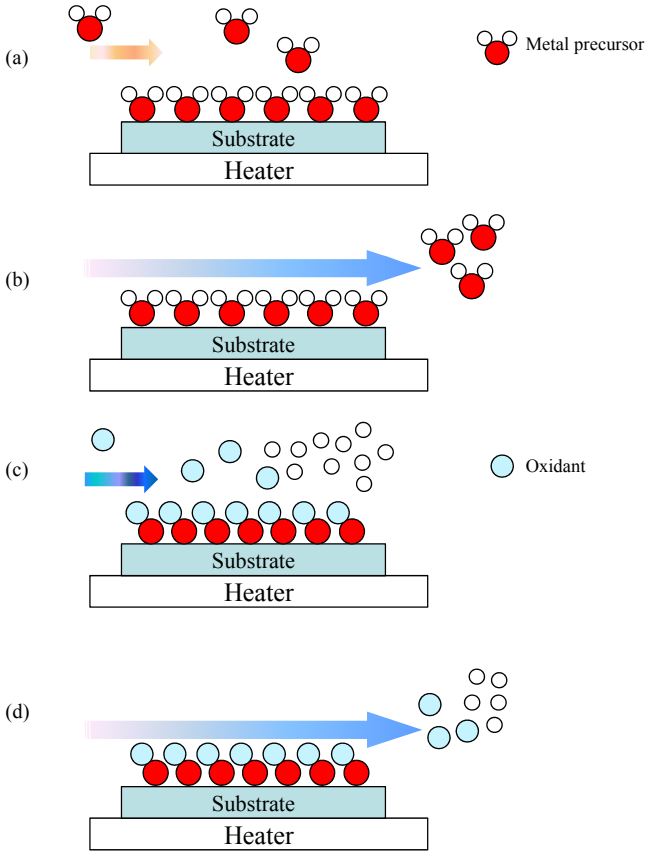

Fig.1 Schematic illustration of one reaction cycle of ALD ZnO film deposition. (a) Metal precursors are introduced and adsorbed onto the surface of substrates. (b) Surplus supply gas is purged by an inert gas (nitrogen). (c) Oxidant is introduced and reacts with metal precursors. (d) Surplus supply gas is purged by an inert gas

In the series of depositions by PAALD, the RF (13.56MHz) plasma was run at 300 W for the films grown in this study. We used diethyl-zinc (DEZ) and trimethyl-aluminium (TMA) as metal precursors for ZnO and Al_2O_3 film depositions, respectively. The charts of the time sequence of PAALD are shown in Fig. 2. The plasma was triggered after the oxygen gas pressure became stable. The plasma ignition time was 1.0 s for the film deposition. [14] The thickness was measured by spectroscopic ellipsometry measurement, and the depth profiles of the films were examined by secondary ion mass spectrometry (SIMS).

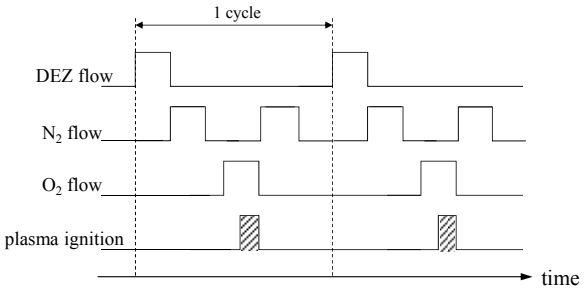

Fig. 2 Charts of the time sequence of PAALD gas supply and plasma ignition.

B. Fabrication of ZnO TFTs

A diagram of the bottom-gate-type ZnO TFTs fabricated in this study is shown in Fig. 3. Fifty-nanometer-thick SiO_2 or Al_2O_3 gate insulators were prepared by thermal oxidation or ALD. Thirty-nanometer-thick ZnO thin films were deposited on p-type Si(100) substrates with the gate insulators by PAALD using DEZ and oxygen radicals at the heater temperature of 100 or 300°C. Ti metal was deposited and patterned by a lift-off technique to serve as the source/drain (S/D) electrodes. The Si substrate was used as the gate electrode.

The channel length (L) and width (W) used in this study were 10 and 20 μm, respectively. The threshold voltage (V_{th}) was defined by the gate voltage (V_g) which induces a drain current of 1 nA at a drain voltage (V_d) of 5 V. The on/off current ratio was measured from the ratio of maximum I_d to minimum I_d on the gate voltage axis.

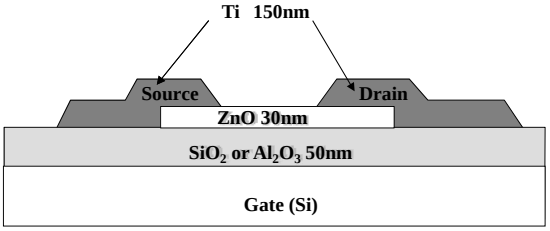

Fig. 3 Schematic of a bottom-gate-type ZnO TFT.

III. RESULTS AND DISCUSSIONS

We deposited ZnO films at 300°C by PAALD on the Si substrate with the gate insulator: TO-SiO_2, Al_2O_3 deposited by conventional ALD (ALD-Al_2O_3) or PAALD (PAALD-Al_2O_3). The transfer characteristics of the fabricated TFTs were measured in single-sweep mode of the gate voltage with V_d = 5 V. Figure 4 shows the variations in the transfer characteristics of the nonannealed ZnO TFTs. All of the TFTs indicated clear TFT behaviors without annealing. The TFT with TO-SiO_2 gate insulator exhibited large negative shift of the V_{th}. This shift of the V_{th} was improved in the case of the TFTs with Al_2O_3 gate insulators, especially, enhancement-type TFTs was obtained by the PAALD-Al_2O_3 gate insulator. It is reported that the flatband voltage (V_{fb}) of Al_2O_3 films deposited by ALD has a tendency to shift toward the positive because of the fixed charge density in the film.[16,17] Therefore, this improvement of the V_{th} shifts seems to be caused by the changes of the Al_2O_3 film properties. [18]

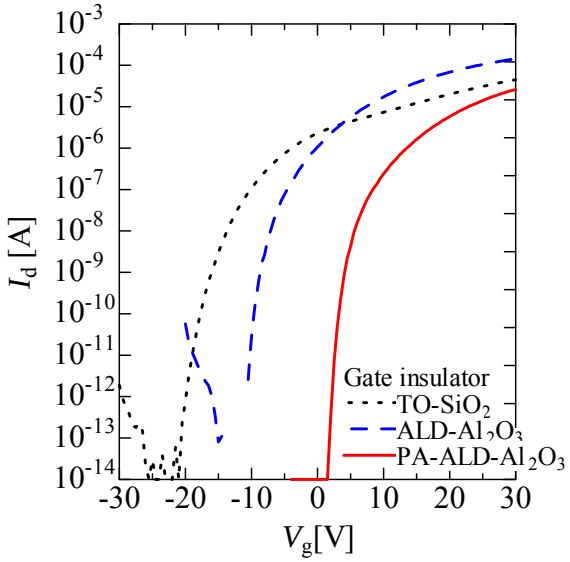

Fig. 4 Variation of the transfer characteristics of the TFTs.

From the results, the high field effect mobility (μ) was obtaind in the case of the TFT with ALD-Al_2O_3 gate insulator. On the other hand, the TFTs with PAALD-Al_2O_3 gate insulator indicated lower off current (I_{d_off}). Therefore, we deposited the five nanometer thick ALD-Al_2O_3 layer on the forty-five nanometer thick PAALD-Al_2O_3 to obtain high TFT performances. For comparison, we fabricated the TFTs with TO-SiO_2 or PAALD-Al_2O_3. We prepared ZnO channel layer and Al_2O_3 gate insulator at 100°C, and the characteristics of the fabricated TFTs were measured without annealing for the low temperature fabrication process. The transfer characteristics of the fabricated TFTs are shown in Fig. 5. All of the TFTs indicated clear TFT device characteristics. In the case of the TFTs with Al_2O_3 gate insulators, higher μ was obtained than that of the TFT with SiO_2 gate insulator. In addition, the TFT with ALD/PAALD stacking Al_2O_3 gate insulator indicated higher performances than the PAALD single layer. The on/off current ratio was > 1×10^9, the μ was 5.1 $cm^2V^{-1}s^{-1}$, and the subthreshold swing was 0.2 V/decade.

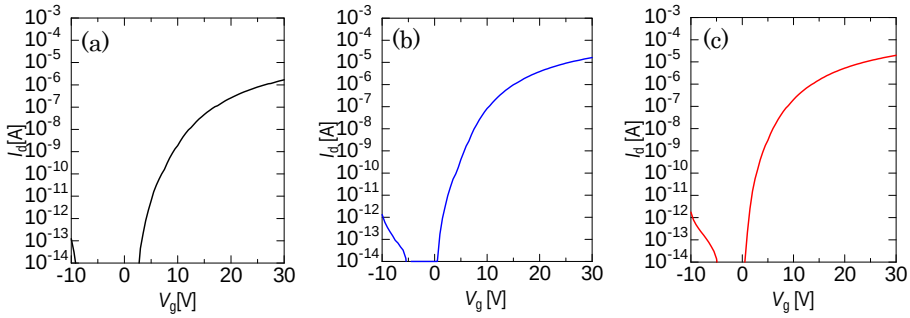

Fig. 5 Transfer characteristics of the ZnO TFTs with (a) SiO_2, (b)PAALD-Al_2O_3 and (c) ALD/PAALD-Al_2O_3 gate insulator. (W/L=20/10mm, V_d=5 V)

In addition, we measured the variation in the transfer characteristics under gate bias stress at room temperature to evaluate device stability. The stressing condition was 20 V of gate voltage. The bias stress was applied for various period of time up to 10000 s. Figures 6(a) and 6(b) respectively show the transfer characteristics before and after stressing periods of 1, 10, 100, 1000, and 10000 s. Figure6(a) shows the bias stress stability of the TFT with thermally-oxidized SiO_2 gate insulator, and Fig. 6(b) shows that of the TFTs with ALD/PAALD stacking Al_2O_3 gate insulator. A large positive shift of V_{th} (ΔV_{th}) was observed after stressing of the TFTs with SiO_2 gate insulator. This V_{th} shift was remarkably reduced in the TFTs with Al_2O_3 gate insulator as shown in Fig. 6(c). From the measurement results of the transfer characteristics, the subthreshold value of the TFT with ALD/PAALD stacking Al_2O_3 gate insulator was improved comparing with that of the TFT with SiO_2 gate insulator. Both subthreshold swing and the stability under the bias stress are affected by the condition of the ZnO/dielectric interface. [19, 20] Therefore, this improvement of the stability seems to be caused by improvement of the ZnO/gate insulator conditions.

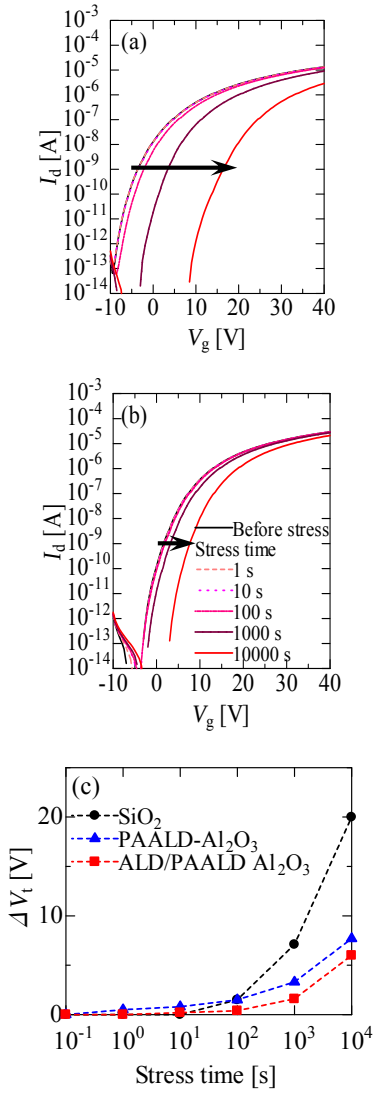

Fig. 6 Variation in transfer characteristics of TFT with (a) SiO_2 and (b) ALD/PAALD-Al_2O_3 gate insulator, and (c) shift of V_{th} under gate bias stress.

We performed SIMS measurement to investigate the change in the ZnO/ gate insulator conditions. Figure 7(a)-(d) show the measurement results of near the interface between the ZnO films and the gate insulators. In the Al_2O_3 film deposited by PAALD shown in Fig. 7 (c), carbon the film considerably decreased comparing with the film deposited by conventional ALD shown in Fig. 7(b). This reduction of carbon suggests that the residual impurities originated from the metal precursor were reduced by the introduction of plasma.[14] In addition, in the samples of ZnO films with ALD-Al_2O_3 film and ALD/PAALD stacking Al_2O_3, increases of the carbon were observed near the ZnO/dielectric interface as shown in Fig.7 (b) and (d). These increases were not observed in the other samples without ALD-Al_2O_3 layer at the ZnO/dielectric interface as shown in Fig. 7 (a) and (b). From these results, the increase of carbon in the ZnO films near the ZnO/dielectric interface is assumed to be due to the presence of mixed layer at the interface. Compared with the transfer characteristics of the TFTs, it is considered that the mixed layer at the interface affects to improve the ZnO TFT device performances.

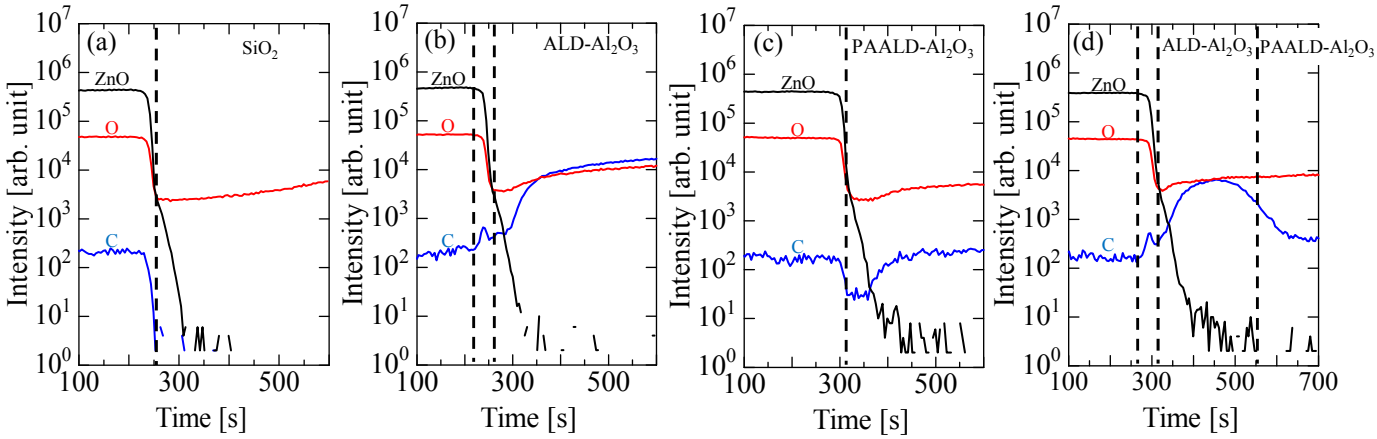

Fig. 7 (Color online) SIMS profiles of ZnO, O, and C in ZnO films with (a) SiO_2, (b) ALD-Al_2O_3, (c) PAALD-Al_2O_3, and (d) ALD/PAALD stacking Al_2O_3 films.

IV. Conclusion

We prepared ZnO and Al_2O_3 thin films deposited by plasma assisted atomic layer deposition in application to an active channel layer and a gate insulator in TFTs. The TFT with Al_2O_3 gate insulator indicated excellent performances without any thermal annealing. The TFT with Al_2O_3 gate insulator deposited by conventional ALD exhibited higher field effect mobility compared with that of the TFT with thermally-oxidized SiO_2 gate insulator. On the other hand, the TFT with Al_2O_3 gate insulator deposited by PAALD indicated lower I_{d_off}. Furthermore, the TFT with PAALD-ZnO channel layer and ALD/PAALD stacked gate insulator deposited at 100°C indicated high-performances, and the stability under the gate bias

stress was improved compared with the TFT with TO-SiO_2 gate insulator. The SIMS measurements suggest that this improvement of the TFT performances seems to be caused by the presence of the mixed layer at the ZnO/dielectric interface. Thorough this study, we confirmed that PAALD makes it possible to obtain the high performance ZnO TFTs at temperatures below 100 degree.

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